(FORM PTO-1390 (REV 11-2000))	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER 124-861
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U S APPLICATION NO (if known, see 37 C F R. 1.5) 09/868241 Unknown
INTERNATIONAL APPLICATION NO. PCT/GB99/04260	INTERNATIONAL FILING DATE 16 December 1999	PRIORITY DATE CLAIMED 19 December 1998

TITLE OF INVENTION

MODIFIED WEIGHTED BIT PLANES FOR DISPLAYING GREY LEVELS ON OPTICAL ARRAYS

APPLICANT(S) FOR DO/EO/US

COKER ~~(et al)~~ Timothy Martin et al

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☒ The U.S. has been elected by the expiration of 19 months from the priority date (Article 31).
5. A copy of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has **NOT** expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 To 20 below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. 3.28 and 3.31 is included.
13. ☐ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821-1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☒ Other items or information. PTO-1449 and copy of International Search Report

U.S. APPLICATION NO (If known, see 37 C.F.R. 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
09/868241 Unknown	PCT/GB99/04260	124-861

21. ☒ The following fees are submitted:

BASIC NATIONAL FEE (37 C.F.R. 1.492(a)(1)-(5):

-- Neither international preliminary examination fee (37 C.F.R. 1.482) nor international search fee (37 C.F.R. 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1000.00

-- International preliminary examination fee (37 C.F.R. 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO.....$860.00

-- International preliminary examination fee (37 C.F.R. 1.482) not paid to USPTO but international search fee (37 C.F.R. 1.445(a)(2)) paid to USPTO.....$710.00

-- International preliminary examination fee (37 C.F.R. 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4).....$690.00

-- International preliminary examination fee (37 C.F.R. 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4).....$100.00

CALCULATIONS PTO USE ONLY							
ENTER APPROPRIATE BASIC FEE AMOUNT =						$	860.00
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(e)).						$	130.00
CLAIMS	NUMBER FILED		NUMBER EXTRA	RATE			
Total Claims	17	-20 =	0	X	$18.00	$	0.00
Independent Claims	5	-3 =	2	X	$80.00		160.00
MULTIPLE DEPENDENT CLAIMS(S) (if applicable)					$270.00	$	270.00
TOTAL OF ABOVE CALCULATIONS =						$	**1420.00**
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.							0.00
SUBTOTAL =						$	**1420.00**
Processing fee of $130.00, for furnishing the English Translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(f)). +							0.00
TOTAL NATIONAL FEE =						$	**1420.00**
Fee for recording the enclosed assignment (37 C.F.R. 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28, 3.31). **$40.00** per property +						$	0.00
Fee for Petition to Revive Unintentionally Abandoned Application ($1240.00 – Small Entity = $620.00)						$	0.00
TOTAL FEES ENCLOSED =						$	**1420.00**
						Amount to be: refunded	$
						Charged	$

a. ☒ A check in the amount of $1420.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. 14-1140 in the amount of $_____ to cover the above fees. A duplicate copy of this form is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 14-1140. A duplicate copy of this form is enclosed.

d. ☒ The entire content of the foreign application(s), referred to in this application is/are hereby incorporated by reference in this application.

NOTE: Where an appropriate time limit under 37 C.F.R. 1.494 or 1.495 has not been met, a petition to revive (37 C.F.R. 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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27,393 REGISTRATION NUMBER

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Imaging Apparatus And Methods

The present invention relates to liquid crystal display apparatus, and to methods of operating a display or spatial light modulator, in which the instantaneous intensity distribution afforded by the display or modulator is binary in nature but which is altered in a manner such that the time averaged distribution effectively has, or appears to have, multiple intensity levels. For display purposes, this means that the alteration must be sufficiently fast for averaging to occur at the eye, preferably avoiding any flicker. This requirement may or may not apply for other purposes.

The methods of the invention can be used in conjunction with any spatial light modulator capable of producing a binary image, including those comprising an array of individually addressable cells or pixels, and those where the binary image is produced by scanning of a modulated light beam, for example. The term " binary spatial light modulator " used herein is intended to encompass all such devices, whether they are used for display or other purposes, for example information recordal, and variable components (for example lenses, filters and diffraction gratings) in optical systems. The term is intended to cover passive modulators where an existing light beam is affected by the modulator, and also those which act as light sources, for example arrays of light emitters, and electroluminescent devices. The apparatus of the invention includes a passive binary spatial light modulator in the form of an array of liquid crystal pixels.

The term "image" as used herein is used to denote any spatially varied light distribution, normally, but not necessarily, of light intensity, and its production or resulting distribution will be referred to by the term "display".

Furthermore, although the term "grey scale" is used herein as denoting a multi-level distribution, it should be made clear that the term is used in relation to any colour, including white. In addition, although the methods, arrays, backplanes, circuitry etc. of the invention and its embodiment are described in relation to a single colour (monochrome images), including white, it is envisaged that variable colour images or displays etc. will be produced in manners known per se, such as by spatially subdividing a single array into different colour pixels, superimposing displays from

differently coloured monochrome arrays for example by projection, or temporal multiplexing, for example sequential projection of red green and blue images.

Temporally varying binary modulation to achieve a multiple intensity effect is known, and can be effected by the use of multiple bit planes. In such a scheme, an array of digitised values, of amplitudes corresponding to the grey scale values allocated to the pixels of the array, is decomposed into a multiplicity of bit planes. This multiple bit plane technique may be used with any binary spatial light modulator as defined above.

It is possible to decompose a n-level grey scale image into a plurality of binary image planes of equal duration, with a corresponding plurality of bit planes of equal duration. However, in a preferred form, known as a weighted bit plane technique, the durations of the bit planes are weighted, each bit plane being representative of one level (exponent) of the digitisation. This reduces the number of bit planes required to synthesise an image, and reduces addressing requirements somewhat. Examples of this technique are to be found in European Patent Application No. 0 774 745 (Matsushita Electronics), and JP 05 127612 (Nippon Hoso Kyokai).

Although in certain cases, it would be possible to use digital bases other than 2, this complicates matters insofar as each bit plane is not binary and thus is not so easily stored. Furthermore, each location of such a bit plane would then have more than one non-zero value, and the variation in non-zero values across the bit plane would need to be taken into account for the durations of operation of each pixel (possibly by further decomposing the non-binary plane to two or more binary planes). The discussion below will be limited to binary weighting, but the principles set out in such a context are believed to be sufficient to enable the skilled person to extrapolate to other exponential bases if required or desired.

Where the digitisation is binary, so that each bit plane is an array of digital 1s and 0s, it is then only necessary to display each bit plane for a total period proportional to its binary weighting to provide a time averaged image equivalent to the digitised grey scale image.

Where possible, it is convenient to display each binary bit plane once for the total duration necessary to contribute to the grey scale image, but it is also possible to display one or more of the bit planes a plurality of times, not necessarily sequentially, provided that the total time spent in displaying each bit plane, relative to the total time spent in displaying all the bit planes, is proportional to its binary weighting.

Recently there has been developed a novel spatial light modulator in the form of a smectic liquid crystal layer disposed between an active semiconductor backplane and a common front electrode. It was developed in response to a requirement for a fast and, if possible, inexpensive, spatial light modulator comprising a relatively large number of pixels (320 x 240 up to 640 x 480) with potential application not only as a display device, but also for other forms of optical processing such as correlation and holographic switching. Depending on the manner in which it is driven, and the value of the applied voltage, the modulator may be driven at a line rate of at least 10MHz and a frame rate of up to 15 to 20kHz, requiring a data input of around 1 to 1.5 Gpixel per second. Typically, while the pixel address time is around 100 nanoseconds, the pixel will actually take around 1 to 5 microseconds to switch between optical states; and while overall frame writing time is of the order of 24 microseconds, the frame to frame writing period is around 80 microseconds.

This spatial light modulator can be driven according to single pass schemes, in which the front electrode is placed at a potential of V/2 relative to the backplane pixels, which are switched to zero volts or V volts.

Alternatively it can be driven according to double pass schemes in which in one pass the front electrode is placed at zero volts and selected pixels are turned ON by switching pixel elements of the backplane array to V volts, and in the other pass the front electrode is placed at V volts and selected pixels are turned OFF by switching elements of the array to zero volts. For pixels which are not in the process of being switched the elements of the backplane follow the voltage of the front electrode. To maintain the same potential difference therebetween, the voltage at all backplane pixel elements of the array is simultaneously switched as the voltage on the front electrode is changed between zero and V volts.

Our copending International Patent Applications (PCT/GB99/04285, ref: P20957WO, priority GB9827952.4; PCT/GB99/04286 and PCT/GB99/04276, refs: P20958WO and P20958WO1, both priority GB9827965.6; PCT/GB99/04282, ref: P20959WO, priority GB9827900.3; PCT/GB99/04279, ref: P20960WO, priority GB9827901.1; PCT/GB99/04274, ref: P20961WO, priority GB9827964.9; PCT/GB99/04275, ref: P20962WO, priority GB9827945.8; and PCT/GB99/04277, ref: P20963WO1, priority GB 9827944.1) relate to other inventive aspects associated with this spatial light modulator, including the single and double pass schemes referred to in the preceding paragraph.

The aforesaid spatial light modulator is ideally suited to the use of the bit plane technique mentioned above. However, the present invention is not limited to liquid crystal modulators, but can be applied to any spatial light modulator as referred to above.

One problem which arises, particularly when operating liquid crystal display and modulators, is that of maintaining a dc balance at individual pixels. Initially, liquid crystal light modulators were in the form of a single cell comprising a layer of liquid crystal material sandwiched between opposed electrode bearing plates, at least one of the plates being transparent. Such cells were slow to operate and tended to have a short life due to degradation of the liquid crystal material. Quite early on it was recognised that the application of an average finite dc voltage to the liquid crystal cell was not beneficial, and at least in some cases produced degradation by electrolysis of the liquid crystal material itself, and schemes were evolved to render the average dc voltage to zero (dc balance).

It is now appreciated that other effects are also at work when a dc voltage is applied. When driving liquid crystal electro-optic devices for any length of time, a phenomenon known as image sticking may occur. Although the precise cause of this effect is unknown, there are theories that ions are trapped or a space charge is induced within the material in response to an overall dc field, and this results in a residual field even when the external dc field is removed.

It is evidently desirable that the time averaged voltage (that is, the average over the time that the voltage is actually being applied from an external source to the liquid crystal) applied to a liquid crystal material is zero, whether to avoid degradation or to avoid image sticking.

The present invention is directed to a weighted bit plane technique as described above in which at least some of the bit planes are modified. It has particular but not exclusive relevance to the production of effective grey scale intensity distributions for display purposes, where the effective duration of the binary images (length and/or number of repeats) is such that temporal integration thereof, for example by a viewer, gives the grey scale image. The methods of the invention find particular but not exclusive application to liquid crystal spatial light modulators.

The different bit planes for a grey scale image can be stored as sequential binary strings in a computer, and will be read out one at a time in any desired order after which they can be discarded unless the image needs to be repeated. It is computationally easiest to read out the bit planes in the order in which they have been stored, since then the only address which needs to be stored is the starting address of the first stored bit planes, all bit planes then being read out one at a time simply by clocking out a predetermined number of data bits in sequence for each bit planes.

It might be possible immediately to replace bit planes that have been read by the bit planes for a succeeding image, particularly where the bit planes are being produced in real time. However, under other circumstances this could be difficult, and the set of bit planes for a successive image will then normally be stored elsewhere. In certain cases it would be possible to provide storage for just two bit planes one of which is written while the other is being read, and vice versa.

It would also be possible to control the reading and/or writing processes so as to convert the image standards as desired, for example from line sequential to interlaced.

As or after each bit plane is read from memory, it is then written, e.g. using the single pass scheme described above, and viewed over a period corresponding to its weighting so that the eye synthesises the intended grey scale image. The single pass

scheme is preferred insofar as it merely over-writes the preceding bit frame without the need for a second pass, the associated front electrode switching and blanking pulses. The avoidance of lost time between successive valid images enables continuous illumination and the easier provision of bit frames of an accurately weighted duration.

In such a scheme, each pixel is subjected to a series of voltage pulses according to the point in the grey scale it represents (as in the number representing the grey scale level, and usually but not necessarily in that order). There are more points in the grey scale than there are applications of voltages, due to the weighting employed, which is advantageous since it reduces the time spent actually driving the array. Each applied voltage may be of the same or opposed polarity compared to the preceding voltage, and the same number of voltage pulses, equal to the number of bit planes (ignoring polarity), is applied to each pixel to synthesise the image.

For example, in a 64 level grey scale with binary weighting, there will be 6 bit planes with relative durations of $2^n t$ where n ranges from 0 to 5, and each pixel can be represented by a corresponding 6 digit binary number.

However, double pass schemes could alternatively be adapted for use in multiple or weighted bit plane schemes.

To achieve dc balance, it would be possible to produce each binary bit plane by any binary imaging method which itself produces dc balance - for example by starting from a blank image, writing, viewing and erasing the binary image by selective energisation (+V) and driven blanking (-V) of selected pixels only.

However, in most or all of such schemes, the actual duration of the binary image is not directly proportional to the time allocated thereto, for example because of intervening blanking steps, etc., leading to a degree of distortion in the binary nature of the bit plane periods, and hence the perceived grey scale values. While this could be compensated for if desired, it represents an additional complication.

The present provides multiple or weighted bit plane apparatus and methods in which dc balance is approached or achieved in ways other than by employing dc balanced

binary images per se, including the alteration of a number or numbers representing pixel intensity. Features and advantages of the invention will become clear upon a reading of the following description, and also upon a perusal of the appended claims to which the reader is directed.

For any selected pixel, each grey scale level can be represented by a binary number, and there are certain binary numbers which possess equal numbers of 0 and 1 digits, for example 111000 and 010101. In these cases the average dc voltage over the 6 bit planes will be zero. Other binary numbers, such as 011000 and 010001 come close to this ideal, and others, in particular 111111 and 000000 are far removed therefrom.

Thus to achieve dc balance in such a scheme, another possibility is (a) to use only those numbers which by themselves achieve dc balance, or (b) at least to alter the grey scale numbers to closely adjacent numbers which closely approach dc balance. This permits use of a single or double pass scheme (see above, and also our copending applications PCT/GB99/04274 and PCT/GB99/04275), addressing all elements during each scan. Some of these schemes per se normally provide no inherent dc balance, and yet in this case dc balance or at least an approximation thereto can be obtained over the grey scale imaging time.

In operation according to the invention in the first instance (a), where the desired grey level differs, it is approximated by the nearest such number in value, for example 000110 becomes 000111, and 100010 becomes 100011. A drawback is that there can be significant distortion of the greyscale.

In the second instance (b), distortion of the greyscale can be reduced but at the expense of precise dc balance. For example, the number 001000 may become 001001, and 110111 may become 110110.

In either instance, unless further corrective steps are taken, extreme values of the grey scale will be omitted (e.g. replaced by an adjacent less extreme value), thus reducing or compressing the contrast range somewhat.

European Patent Application Serial No. 0 720 139 (Pioneer Electronic Corporation) discloses a method for correcting grey scale data for a weighted bit plane technique in

which the numbers indicative of pixels intensity are altered in a manner intended to prevent false contouring which otherwise arises in a self luminous display, such as an electroluminescent or plasma display. In such a case, the alteration at any pixel can reduce, maintain or increase the inequality of 1s and 0s, and in the latter case dc balance will deteriorate further, and it is believed that false contouring is a problem peculiar to self-luminescent displays, as opposed to passive liquid crystal displays.

In a first aspect the invention provides a method of image signal processing for a weighted bit plane technique, in which an image signal represents a set of n-digit binary number signals each indicative of the intended intensity level of a respective one of a corresponding array of binary pixels, wherein at least one said binary number has an inequality of 1s and 0s, characterised in that said method comprises the step of altering the said at least one binary number to a closely adjacent value to reduce or remove the said inequality therein and so that any inequality of 1s and 0s in each of said set of numbers is left unchanged, reduced or removed.

In a second aspect the invention provides a method of writing and displaying an image in response to an image signal representing a set of n-digit binary numbers each indicative of the intended intensity level of a respective one of a corresponding array of binary pixels, a complete image being written using a weighted bit plane technique, the method being characterised in that at least one said binary number is altered to a closely adjacent value such that over the writing of said complete image an inequality of 1s and 0s at the corresponding pixel is reduced or removed and so that any inequality of 1s and 0s at pixels for each of the rest of the said set of numbers is left unchanged, reduced or removed.

The methods according to the first and second aspects of the invention (and also that of the fourth aspect - see below) is in fact particularly useful when driving an array of liquid crystal pixels.

In a third aspect the invention provides light modulating apparatus comprising an array of light modulating pixels and drive means adapted to drive the array to write a complete image by a weighted bit plane technique in response to an image signal

representing a set of n-digit binary numbers defining the intended intensities of respective pixels of the array, n being an integer greater than one,

characterised in that the pixels are liquid crystal pixels, and the driving means is arranged to alter the n-digit number in respect of at least one said pixel to a closely adjacent value so that the numbers of 1s and 0s written thereat over said writing of a complete image are brought closer to equality whereby to improve the dc balance.

In the weighted bit plane technique the driving means may provide from the image signal a group of n binary bit plane signals each representative of a respective digit from each of the set of numbers, i.e. a respective exponent of digitisation, and write the display with each bit plane signal at least once in a predetermined sequence and with predetermined timings to thereby write a complete image with integrated pixel intensities substantially corresponding to said image signal.

In a refinement, time averaging of both dc and grey scale level is performed over more than one frame, by suitable choice of the binary numbers. In this manner, dc balance can be closely approximated, or preferably attained, while the average grey scale level can be approximated or, preferably, maintained. For example, 110110 (27) could be replaced by 001110 (28) in a first frame and by 010110 (26) in second frame. The average grey scale level is 27 as desired, and both the binary numbers actually used provide dc balance per se.

In a more complicated example, the grey scale level 15 (111100) could be used twice together with an additional frame for grey level 14 (011100) and another additional frame for grey level 16 (000010), the frames in any desired order. Over the four frames the average grey level is 15, and there are equal numbers of binary 1s and 0s.

Accordingly in a fourth aspect the invention also provides a method of writing and displaying an image in response to an image signal representing a set of n-digit binary numbers each indicative of the intended intensity level of a respective one of a corresponding array of binary pixels, using a weighted bit plane technique, wherein at least one said binary number produces an inequality of 1s and 0s at its pixel over the writing of a complete image, characterised in that a plurality of images each approximating said complete image are written in succession, and the said at least one

binary number is altered to a closely adjacent value in at least one of said plurality of images so that over said succession the said inequality of 1s and 0s is reduced or removed and any inequality of 1s and 0s at each of the other pixels is left unchanged, reduced or removed. Preferably the inequality in said at least one pixel is eliminated. The average intensity over the plurality of images is at least approximated, but preferably maintained.

In a fifth aspect the invention provides light modulating apparatus comprising an array of light modulating pixels and drive means adapted to drive the array to write a complete image by a weighted bit plane technique in response to an image signal representing a set of n-digit binary numbers defining the intended intensities of respective pixels of the array, n being an integer greater than one,

characterised in that the pixels are liquid crystal pixels, and over a plurality of successive said complete images the driving means is arranged to alter the n-digit number in respect of at least one said pixel in at least one said complete image to a closely adjacent value so that the numbers of 1s and 0s written at said at least one said pixel over the plurality of images are brought closer to equality whereby to improve the dc balance.

Again extremes of the grey scale are preferably omitted. If in either case, the full grey scale ranges are retained, dc balance can be periodically restored by other means, for example by applying corrective dc pulses as appropriate following a computer simulation of the dc imbalance which has accumulated, as mentioned above. However, this is not normally preferred, since it potentially involves using a number of corrective dc pulses equal in number to the number of bit planes which have been used, to allow for the possibility that at least one pixel has remained at an extreme grey scale value throughput the imaging period.

These ways of maintaining dc balance in grey scale imaging arise at least in part from the reduction in number of address steps compared with the number of grey scale levels. One way of deriving the grey scale value or combinations of grey scale values for use in operation of the multiple or weighted bit plane scheme, that is, replacing the

input grey scale value derived from the intended image itself, is by means of a look-up table.

The weighted bit plane method as operated above does require that relaxation of the pixels is negligible over the duration of the longest bit plane, and this is not always possible, particularly in the case of liquid crystal pixels. In such a case, the bit planes can be refreshed during the bit plane period(s), but at the possible expense of dc balance. Nevertheless there are advantages in the ease of obtaining an accurately simulated grey scale.

Basically, a refresh step comprises repeating the application of the same voltage as was applied at the start of the bit plane so as to restore the switched state of the pixel. It may even be that the nth power binary weighted bit plane needs to be refreshed $(2^{n-1}-1)$ times subsequent to the first writing so that a $(2^n - 1)$ greyscale will involve 2^{n-1} frame writes of binary images when the refresh writing stages are included. However, the increasing number of writing steps makes it increasingly difficult to alter the bit frames according to the invention in the direction of providing dc balance, and in the limit of 2^{n-1} frame writes (where the lowest order bit plane is the only one not refreshed), the present invention cannot be successfully applied.

However, there will be occasions where refreshing is only necessary with the longer duration bit planes. In such a case it would be again be possible to practice a method according to the present invention, using the actual binary numbers describing the pixel as previously described. However, a preferred method according to the invention is practised by taking determining the aggregate of the 1s and 0s occurring over the whole frame (single image method) or frames (plural image method), including the refreshed values, and altering the number for a pixel having an inequality of 1s and 0s so determined as to reduce the inequality. That is, that this preferred method acts on the binary numbers for each pixel as expanded according to the need to refresh.

For example, taking a simple example of pixels represented by a binary number comprising only four digits per pixel, where the first two, higher order, digits need to be refreshed, but the 3rd and 4th can be displayed without the need to refresh, it will

be necessary to refresh the longest bit plane four times and the next longest twice. Taking the number 1001, this then becomes (1111)(00)01, where the brackets demarcate the original digits, having 5 unit values but only three zeros. Conversion of the original number to 1000 gives equality of values in the expanded number (11110000).

In the refresh scheme, bit planes are read out more than once, depending on the duration thereof. Thus it is not possible to discard the bit plane until it has undergone its final reading. Furthermore, if each bit plane is repeatedly read for the requisite number of times before proceeding to the next bitframe, it is necessary to store the starting address of the two bit planes.

For example, taking a simple case of three bit planes A, B and C, of relative durations 4t, 2t and t respectively, it would be possible to read these out in the order AAAABBC. However, this necessitates storing the start addresses of each of the bit planes, apart from frame C which is read only once, in order that the correct place for the refresh readout may be reached.

In addition, and perhaps more importantly, there are cases where it is necessary to rewrite the entire grey scale image before proceeding to a new image, where display times are long or relaxation is fast for example. In such a case it is necessary not only to store the start address of the bit plane next to be used, but also the start address of the first bit plane of the entire sequence, until that image information is no longer required.

An improved method of readout in such cases makes it possible to avoid the storage of a plurality of start addresses. At the high speeds involved in reading out the images when using the spatial light modulator of the preferred embodiment, this apparently minor step can be computationally significant and advantageous.

Essentially, a plurality of the highest order bit planes (or all the bit planes), are stored as binary strings in sequential locations in a memory, in decreasing order of intended duration (weighting), a predetermined number of read passes are made from the set of stored bit planes equal to the plurality of weighted bit planes, each pass commencing

with the highest order bit plane and continuing along the stored bit planes in sequence, the lengths of the sequences being selected and varied such that at the end of the predetermined number of read passes each bit frame has been read out a plurality of times proportional to or equal to its duration (weighting). This general method of fast readout forms the subject of our copending International Patent Application No. PCT/GB99/04277 filed on the same day as this application.

Thus according to this scheme, the triple bitframe image exemplified above will be read out with read passes ABC (once), AB (once), and A (twice), which when combined can give an overall order, for example, of ABCABAA, or ABCAAAB or ABAAABC as desired. Only the start address needs to be stored since each read pass commences at the same place, and continues to an address determined by counters.

Where grey scale imaging is practised according to the invention, but with refreshing of a plurality of the highest order bit planes, it is possible to apply this fast readout method to the set comprising the bit planes which are refreshed plus the next lowest order bit plane. Any remaining lower order bit plane(s) which are not refreshed will be read out once, for duration(s) less than the lowest order bit plane of the set according to their weighting. This can be done at any time, including a period or periods within the reading out of the plurality, but is preferably performed before or after the entire set has undergone a fast readout.

While some of the grey scale and refresh schemes above automatically provide dc balance, a further option for schemes which do not do this is to allow dc imbalance to accumulate, for example while writing images and then allowing them to relax, calculating the imbalance (e.g. in an accompanying computer simulation), and then applying local dc voltages to the pixels of a magnitude and duration such as to provide zero average dc.

It should be understood that there have been references above to a liquid crystal cell incorporating an addressable array, the methods of the invention may be used in relation to any binary spatial light modulator. Where the imaging device is a liquid crystal device, prolongation of the binary images used to synthesise the grey scale

image may be achieved in known manner by the application of a small ac field between successive binary images.

CLAIMS

1. Light modulating apparatus comprising an array of light modulating pixels and drive means adapted to drive the array to write a complete image by a weighted bit plane technique in response to an image signal representing a set of n-digit binary numbers defining the intended intensities of respective pixels of the array, n being an integer greater than one,

characterised in that the pixels are liquid crystal pixels, and the driving means is arranged to alter the n-digit number in respect of at least one said pixel to a closely adjacent value so that the numbers of 1s and 0s written thereat over said writing of a complete image are brought closer to equality whereby to improve the dc balance.

2. Light modulating apparatus comprising an array of light modulating pixels and drive means adapted to drive the array to write a complete image by a weighted bit plane technique in response to an image signal representing a set of n-digit binary numbers defining the intended intensities of respective pixels of the array, n being an integer greater than one,

characterised in that the pixels are liquid crystal pixels, and over a plurality of successive said complete images the driving means is arranged to alter the n-digit number in respect of at least one said pixel in at least one said complete image to a closely adjacent value so that the numbers of 1s and 0s written at said at least one said pixel over the plurality of images are brought closer to equality whereby to improve the dc balance.

3. Display apparatus according to claim 2 wherein said driving means is arranged so that values of said number over said plurality of images provide an average intensity at said at least one pixel substantially equal to the intended intensity.

4. Display apparatus according to claim 2 or claim 3 wherein said plurality of images is two or four images.

5. Display apparatus according to any preceding claim wherein said driving means is arranged so that said numbers of 1s and 0s written at said at least one said pixel are brought to equality.

6. Display apparatus according to any preceding claim wherein said driving means includes a look-up table for determining how said at least one number is to be altered.

7. Display apparatus according to any preceding claim wherein said driving means is arranged so that at least the weighted bit plane corresponding to the most significant digit of the numbers in said set is refreshed during the writing of said complete image.

8. Display apparatus according to claim 7 wherein said driving means is arranged so that a plurality m of the weighted bit planes corresponding to a like plurality of the most significant digits of the numbers in said set are refreshed during the writing of a complete image, where m is a positive integer at least 2 lower than n, and said driving means includes a memory and means for storing in said memory signals for the first plurality of bit planes as a corresponding first plurality of binary strings in sequential locations in said memory in decreasing order of significance of said significant digits, the drive means further including means arranged to make a succession of read cycles from the stored strings, each read cycle consisting of reading one or more of the stored strings in sequence as stored, commencing with the string for said most significant digit, the numbers of the strings read in the read cycles being varied so that at the end of the said succession of read cycles each string of the first plurality has been read out a plurality of times proportional to the exponent of its associated digit.

9. Display apparatus according to claim 8 wherein said storing means is arranged to store all of the bit plane signals as strings in sequential locations in said memory in decreasing order of significance of the associated digit.

10. Display apparatus according to claim 8 or claim 9 wherein said driving means is arranged to write bit planes not in said plurality once per said succession for periods determined by the exponents of their associated digits.

11. Display apparatus according to any preceding claim and including means for applying a small ac potential difference to pixels of the array in periods when bit planes are not being written to prolong the display.

12. A method of image signal processing for a weighted bit plane technique, in which an image signal represents a set of n-digit binary number signals each indicative of the intended intensity level of a respective one of a corresponding array of binary pixels, wherein at least one said binary number has an inequality of 1s and 0s, characterised in that said method comprises the step of altering the said at least one binary number to a closely adjacent value to reduce or remove the said inequality therein and so that any inequality of 1s and 0s in each of the rest of the said set of numbers is left unchanged, reduced or removed.

13. A method of writing and displaying an image in response to an image signal representing a set of n-digit binary numbers each indicative of the intended intensity level of a respective one of a corresponding array of binary pixels, a complete image being written using a weighted bit plane technique, the method being characterised in that at least one said binary number is altered to a closely adjacent value such that over the writing of said complete image an inequality of 1s and 0s at the corresponding pixel is reduced or removed and so that any inequality of 1s and 0s at pixels for each of the rest of the said set of numbers is left unchanged, reduced or removed.

14. A method of writing and displaying an image in response to an image signal representing a set of n-digit binary numbers each indicative of the intended intensity level of a respective one of a corresponding array of binary pixels, using a weighted bit plane technique, wherein at least one binary number produces an inequality of 1s and 0s at its pixel over the writing of a complete image, characterised in that a plurality of images each approximating said complete image are written in succession, and the said at least one binary number is altered to a closely adjacent value in at least one of said plurality of images so that over said succession the said inequality of 1s and 0s is reduced or removed and any inequality of 1s and 0s at each of the other pixels is left unchanged, reduced or removed.

15. A method according to claim 13 or claim 14 wherein at least one bit plane is refreshed during the writing of a said complete image.

RULE 63 (37 C.F.R. 1.63)
DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Modified Weighted Bit Planes for Displaying Grey Levels on Optical Arrays

the specification of which (check applicable box(es))

- ☐ is attached hereto
- ☐ was filed on _____ as U S. Application Serial No _____
- ☒ was filed as PCT international application No. PCT/GB99/04260 on 16/12/1999

and (if applicable to U.S. or PCT application) was amended on 05/01/2001

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 C.F.R. 1.56. I hereby claim foreign priority benefits under 35 U S.C. 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed or, if no priority is claimed, before the filing date of this application:

Priority Foreign Application(s):

Application Number	Country	Day/Month/Year Filed
9827944.1	GB	19/12/1998

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below.

Application Number	Date/Month/Year Filed

I hereby claim the benefit under 35 U.S.C. 120/365 of all prior United States and PCT international applications listed above or below and, insofar as the subject matter of each of the claims of this application is not disclosed in such prior applications in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose material information as defined in 37 C F.R. 1.56 which occurred between the filing date of the prior applications and the national or PCT international filing date of this application:

Prior U.S./PCT Application(s): Application Serial No.	Day/Month/Year Filed	Status: patented pending, abandoned
PCT/GB99/04260	16/12/1999	PENDING

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon And I hereby appoint **NIXON & VANDERHYE P.C., 1100 North Glebe Rd., 8th Floor, Arlington, VA 22201-4714, telephone number (703) 816-4000 (to whom all communications are to be directed)**, and the following attorneys thereof (of the same address) individually and collectively my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent. Arthur R. Crawford, 25327; Larry S. Nixon, 25640, Robert A Vanderhye, 27076; James T Hosmer, 30184; Robert W. Faris, 31352; Richard G. Besha, 22770; Mark E. Nusbaum, 32348, Michael J Keenan, 32106; Bryan H. Davidson, 30251; Stanley C. Spooner, 27393; Leonard C. Mitchard, 29009; Duane M. Byers, 33363; Jeffry H Nelson, 30481; John R. Lastova, 33149; H. Warren Burnam, Jr. 29366; Thomas E. Byrne, 32205; Mary J Wilson, 32955; J Scott Davidson, 33489; Alan M. Kagen, 36178; William J. Griffin, 31260; Robert A. Molan, 29834; B. J. Sadoff, 36663; James D. Berquist, 34776; Updeep S. Gill, 37334; Michael J. Shea, 34725, Donald L. Jackson, 41090; Michelle N. Lester, 32331.

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FOR ADDITIONAL INVENTORS, check box ☒ and attach sheet with same information and signature and date for each.

RULE 63 (37 C.F.R. 1.63)
DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Modified Weighted Bit Planes for Displaying Grey Levels on Optical Arrays

the specification of which (check applicable box(s)).

- ☐ is attached hereto
- ☐ was filed on _____ as U.S Application Serial No _____
- ☒ was filed as PCT international application No. PCT/GB99/04260 on 16/12/1999
- and (if applicable to U.S. or PCT application) was amended on 05/01/2001

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 C.F.R. 1.56. I hereby claim foreign priority benefits under 35 U.S C. 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed or, if no priority is claimed, before the filing date of this application:

Priority Foreign Application(s):

Application Number	Country	Day/Month/Year Filed
9827944.1	GB	19/12/1998

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below.

Application Number	Date/Month/Year Filed

I hereby claim the benefit under 35 U.S.C 120/365 of all prior United States and PCT international applications listed above or below and, insofar as the subject matter of each of the claims of this application is not disclosed in such prior applications in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. 1.56 which occurred between the filing date of the prior applications and the national or PCT international filing date of this application.

Prior U.S./PCT Application(s): Application Serial No.	Day/Month/Year Filed	Status: patented pending, abandoned
PCT/GB99/04260	16/12/1999	PENDING

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. And I hereby appoint **NIXON & VANDERHYE P.C., 1100 North Glebe Rd., 8th Floor, Arlington, VA 22201-4714, telephone number (703) 816-4000 (to whom all communications are to be directed),** and the following attorneys thereof (of the same address) individually and collectively my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent: Arthur R. Crawford, 25327; Larry S Nixon, 25640; Robert A. Vanderhye, 27076; James T. Hosmer, 30184; Robert W. Faris, 31352; Richard G. Besha, 22770; Mark E Nusbaum, 32348, Michael J. Keenan, 32106; Bryan H. Davidson, 30251; Stanley C. Spooner, 27393, Leonard C. Mitchard, 29009; Duane M. Byers, 33363; Jeffry H. Nelson, 30481, John R Lastova, 33149; H. Warren Burnam, Jr 29366; Thomas E. Byrne, 32205; Mary J. Wilson, 32955; J Scott Davidson, 33489; Alan M. Kagen, 36178; William J. Griffin, 31260; Robert A. Molan, 29834, B. J. Sadoff, 36663, James D. Berquist, 34776; Updeep S. Gill, 37334, Michael J Shea, 34725; Donald L. Jackson, 41090; Michelle N. Lester, 32331.

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FOR ADDITIONAL INVENTORS, check box ☒ and attach sheet with same information and signature and date for each.